

Appln No. 09/611,809

Amdt date December 27, 2004

Reply to Office action of September 24, 2004

**REMARKS/ARGUMENTS**

In the final Office action dated September 24, 2004 the Examiner rejected claims 1 - 20 under 35 U.S.C. § 103(a) as being unpatentable over Hobson et al. (U.S. Patent No. 6,209,016). By this amendment and the accompanying Request for Continued Examination Applicant has amended claims 1 - 3 and added claims 21 and 22. Accordingly, claims 1 - 22 are now presented for Examination. Claims 1, 21 and 22 are independent claims. Claims 2 - 20 depend on claim 1.

Amended claim 1 recites, in part: "at least one adder and at least two multipliers configurable to perform specified multiplication operations in parallel and configurable to perform specified multiplication and addition operations in parallel" and "a decode unit . . . configured to issue instructions so that the execution unit performs specified multiplication and addition operations in parallel and performs specified multiplication operations in parallel."

In contrast, Hobson et al. does not teach or suggest an encryption processor where instructions are issued to cause specific multiplication and addition operations to be performed in parallel and to cause specific multiplication operations to be performed in parallel.

At paragraph 3 of the Office action the Examiner cites Hobson et al. at column 8, lines 20 - 43 as teaching that "certain multiply or addition [operations] are performed in parallel while performing either the square of product operation." However, this passage simply states that "operations (1), (2), (3), (4), (5) and (7) are all modular

**Appln No. 09/611,809**

**Amdt date December 27, 2004**

**Reply to Office action of September 24, 2004**

operations that use the Montgomery Algorithm and use the co-processor as a modular multiplier" and that "[s]tage (8) uses the ordinary multiply function, whilst stages (6) and (9) make use of the new arithmetic operations . . . namely, addition and subtraction." This passage does not, however, teach or suggest the specific structure and combination of operations provided by the apparatus of claim 1 as outlined above for example.

Moreover, the invention of claim 1 provides an efficient method of performing an operation on an operand by performing specified operations in parallel. The portion of column 4 in Hobson et al. cited by the Examiner at paragraph 4.2 of the Office action teaches splitting a serial bit stream "into two (odd and even) component bit streams (bits from the originating serial bit stream are fed alternately into the two component bit streams respectively) and the two component bit streams are processed in parallel, one bit being presented by each of the component bit streams at the same time to form a bit-pair for calculation." Thus, all addition, subtraction and multiplication operations are performed in parallel on alternating bits of data from a serial data stream. Consequently, Hobson et al. does not teach or suggest the use of instructions to cause specified operations to be performed in parallel.

In view of the above, Applicant submits that the invention of claim 1 is not obvious in view of Hobson et al. Claims 2 - 20 that depend on claim 1 also are patentable over the cited references for the reasons set forth above. In addition, these

**Appln No. 09/611,809**

**Amdt date December 27, 2004**

**Reply to Office action of September 24, 2004**

dependent claims are patentable over these references for the additional limitations that the dependent claims contain.

New claim 21 includes limitations relating to, for example, "performing, by an execution unit, simultaneous multiplication operations in response to at least one of the first instruction and the second instruction; and performing, by the execution unit, simultaneous multiplication and addition operations in response to at least one of the first instruction and the second instruction."

New claim 22 includes limitations relating to, for example, "issuing, by the decode unit, a first set of instructions for an execution unit to perform the Montgomery square operation, the first set of instructions comprising: a first instruction to perform simultaneous multiplication operations; and a second instruction to perform simultaneous multiplication and addition operations."

For reasons similar to those discussed above, Hobson et al. does not teach or suggest all of the limitations of claim 21 or claim 22.

Appln No. 09/611,809

Amdt date December 27, 2004

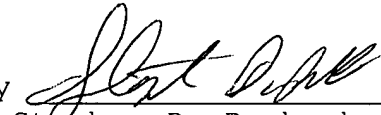
Reply to Office action of September 24, 2004

#### CONCLUSION

In view of the above amendment and remarks it is submitted that the claims are patentably distinct over the cited references and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Respectfully submitted,  
CHRISTIE, PARKER & HALE, LLP

By



Stephen D. Burbach

Reg. No. 40,285

626/795-9900

SDB/sdb

SDB PAS600241.1-\*--12/27/04 5:44 PM